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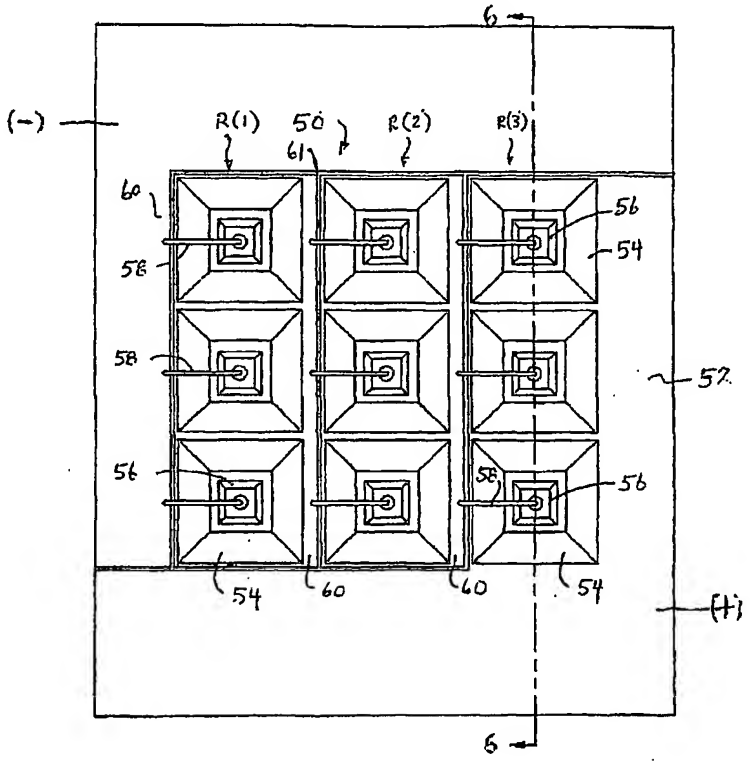
(54) Title: MICRO-REFLECTORS ON A SUBSTRATE FOR HIGH-DENSITY LED ARRAY



(57) Abstract: The present invention provides an optical array module (50) that includes a plurality of semiconductor devices (56) mounted on a thermal substrate formed with a plurality of openings that function as micro-reflectors, wherein each micro-reflector includes a layer of reflective and conductive material (62) to reflect light and to electrically power its associated semiconductor device.

WO 2005/091392 A1

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MICRO-REFLECTORS ON A SUBSTRATE FOR HIGH-DENSITY LED ARRAY

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Related Applications

This application claims priority from U.S. Provisional Application Serial Number 60/554,628, filed March 18, 2004, the contents of which are hereby incorporated by reference as recited in full herein for all purposes.

Background of the Invention

This invention relates to high-density LED arrays and, more particularly, to a lower cost LED array that has improved collection and collimation of light.

High-density UV LED arrays may be used for curing applications ranging from ink printing to the fabrication of DVDs and lithography. Many such applications require a high optical power density at the working surface. However, light distribution from a typical LED is highly divergent. For example, Fig. 1 is a graphic illustration showing radiation distribution for two different LEDs 22, 24 mounted on a surface 26 without refractive or reflective optics. Ideally, for such applications, the light from an LED would be distributed substantially 90 degrees from substrate 26. However, typical LEDs emit highly divergent light. Curve 28 is a representative example of radiation distribution from first LED 22 and curve 30 is a representative example of radiation distribution from second LED 24. As can be seen, much of the optical radiation from the LEDs 22, 24 is emitted at highly oblique angles. This causes the optical power density to fall off quickly as a function of the distance of the work surface from the LED, which is graphically illustrated in Fig. 2 for an LED array without refractive or reflective optics. The illustrations of Figs. 1

and 2 would be different for different LEDs and different arrays and would depend on the number and spacing of LEDs in the array. To achieve the required optical power density the LED array must often be located physically closer to the work surface than is desired necessitating mechanical changes to tooling and/or shielding to accommodate its near proximity. However, locating the LED array too far from the work surface may diminish the optical power density to undesired levels.

There are known methods of achieving higher optical power density. For example, some LEDs are used with Lambertian optical outputs to achieve a higher optical power density. However, such devices are less efficient in electrical to optical conversions as well as being less thermally efficient. Another method of achieving higher optical power density is shown if Fig. 3 in which an array of refractive optical elements 32 is located above an array of LEDs 34 in which each LED 34 is associated with an optical element 32. Each optical element 32 collects and collimates the light from its associated LED 34. However, this method is inefficient because light from LEDs is highly divergent causing much of the light to fall outside the numerical aperture of the lenses. The numerical aperture of a lens is defined as the sine of the angle between the marginal ray (the ray that exits the lens system at its outer edge) and the optical axis multiplied by the index of refraction (n) of the material in which the lens focuses. In order to more effectively collect and collimate the light the optical component must have a very high numerical aperture resulting in a lens that has a very large diameter and a very short focal length. In practice, it is not possible to manufacture a refractive optical element that collects all of the light from an LED because that would require the angle between the optical axis and the marginal ray to be 90 degrees, implying a lens of either a zero focal length or an infinite diameter.

Another common approach to collecting and collimating light from an LED is

to use a parabolic reflector as shown in Fig. 4. An LED 36 is mounted in parabolic reflector 38 so that light rays 40 emitted from LED 36 are collected and collimated. For example, a typical application of such refractive optics is with LED-mounted flashlights in which the refractive optic collimates light from only a single LED. Unlike reflective optics, reflective optics can easily collect all the light from the LED even at very highly oblique angles. However, known reflective optics are not capable of being used in a tightly packed or dense array because of their size. Furthermore, macro-reflectors that are larger than an optical array are not as optically efficient as the micro-reflectors of this invention.

Additionally, in known optical devices the reflector is separate from the electrical circuitry of the device. For example, such devices typically utilize a macro-reflector for an entire array of LEDs. The optical efficiency of these devices is lowered because each LED does not have an associated reflector. Furthermore, the separate reflector increases the cost of manufacturing. Additionally, the volume of space required for the macro-reflector is very large making it less useful for some applications.

Summary of the Invention

The present invention provides a low-cost LED optical array to better collect and collimate light from an LED array. The improved collection and collimation of the LED light allows the LED array to be physically located further away from a work surface yet maintain high optical power.

The present invention provides a very dense LED array in which individual LEDs are mounted on a substrate formed to incorporate an array of micro-reflectors. Preferably, the substrate is of a material that is electrically insulating and thermally

conductive. The substrate is formed with micro-reflectors within which one or more LEDs are mounted. In one preferred embodiment, the substrate is anisotropically etched to form micro-reflectors having a substantially truncated pyramidal shape. Preferably, the substrate is a crystalline silicon having defined crystallographic axes along which the substrate is etched to form openings in the substrate having walls with a characteristic slope. The openings are the metallized and structured to define separate circuits. The resulting substrate has openings formed in a dense array, which openings are then coated with a reflective and electrically conductive material so that the openings function both as electrical connections and as micro-reflectors. The substrate is then assembled LEDs mounted within each micro-reflector and wired into a circuit on the substrate. The array is then electrically connected to a power source. The substrate may be formed of any size and the LEDs arranged in any desired dense configuration required for a particular application.

In another preferred embodiment, a very dense LED array is provided in which an array of parabolic micro-reflectors is formed in a substrate of silicon or other thermally conductive semiconductor and ceramic materials such as diamond, SiC, AlN, BeO, Al2O3, or combinations of these with other materials. The parabolic micro-reflectors can be laser and/or plasma machined into the substrate. Other patterned or alternatively shaped micro-reflectors may be formed in the substrate to direct light from LEDs by reflection.

In another preferred embodiment, micro-reflectors may be formed in a substrate by a combination of etching and machining. For example, a substrate may be etched to form openings having a characteristically sloped wall. The substrate may then be coated with a reflective material. Each opening may then machined to have a desired shape such as a parabolic shape.

The present invention provides an array module that includes a plurality of semiconductor devices mounted on a thermal substrate formed with a plurality of openings that function as micro-reflectors, wherein each semiconductor device or multiple devices is associated with a micro-reflector, each micro-reflector including a layer of reflective and conductive material to reflect light and to electrically power its associated semiconductor device.

The present invention further provides a method of manufacturing an array module comprising the steps of providing a substrate, forming a plurality of openings in the substrate, providing a layer of reflective and electrically conductive material in each opening, and mounting a semiconductor device within each opening so that the layer of reflective and electrically conductive material in each opening reflects light and electrically powers from its associated semiconductor device.

The present invention provides for an alternative method of manufacturing an array module in which a substrate material is metallized. Metal circuits are then structured on the metallized substrate and the substrate is then etched to form openings. The openings are then metallized to form micro-reflectors that both reflect light and electrically power a semiconductor device. This has the advantage of allowing fine features to be formed in the electrical circuit separately from the etching and plating tasks associated with forming the micro-reflectors.

The present invention further provides an optical device that incorporates a reflector into the electrical circuitry of the optical device to obtain higher optical efficiency with lower costs.

These and other embodiments are described in more detail in the following detailed descriptions and the figures.

The foregoing is not intended to be an exhaustive list of embodiments and

features of the present invention. Persons skilled in the art are capable of appreciating other embodiments and features from the following detailed description in conjunction with the drawings.

Brief Description of the Drawings

Figure 1 shows radiation distribution for two LEDs without refractive or reflective optics.

Figure 2 shows a graph of an example of power drop-off as a function of distance from the LED array for a specific array.

Figure 3 shows an example of prior art refractive lenses used to collect and collimate light from an array of LEDs.

Figure 4 shows a common approach of collecting and collimating light from an LED with a parabolic reflector.

Figure 5 is an enlarged top view of a portion of an LED array according to one aspect of the present invention.

Figure 6 is a view of the LED array of Figure 5 taken along line 6-6.

Figure 7 is a top view of the substrate formed with an array of pockets according to one aspect of the invention.

Figure 8 is an enlarged partial top view of a portion of the substrate of Figure 7.

Figure 9 is an enlarged partial side view of a portion of the substrate of Figure 7.

Figure 10 is a graphic illustration showing the improved directionality of light from an LED with reflective pockets of the substrate of the invention.

Figure 11 is a graph of calculated power as a function of distance for an LED array arranged on a grid with 1 mm center-to-center spacing.

Figure 12 is an alternative embodiment of the invention with parabolic micro-reflectors.

Figure 13 is yet another embodiment of the invention in which the micro-reflectors are formed by a combination of etching and machining.

Figure 14 is another embodiment of the invention incorporating an array of micro-lenses.

Detailed Description of the Invention

Representative embodiments of the present invention are shown in Figs. 5-14, wherein similar features share common reference numerals.

Figure 5 shows a portion of a high-density LED array 50 that may be used for applications requiring high optical power density at the working surface. Such applications may include, for example, curing applications ranging from ink printing to the fabrication of DVDs and lithography. One such high-density LED array is shown and described in U.S. Patent Application No. 10/984,589, filed November 8, 2004, the entire contents of which are hereby incorporated by reference for all purposes. Array 50 includes a substrate 52 having micro-reflectors 54 formed therein. An LED 56 is mounted within each micro-reflector 54 in a manner known by those skilled in the art. Although the figures show only one LED associated with a micro-reflector each micro-reflector may be associated in one or more LEDs, such as one of each red, green, and blue or any combination thereof. One type of LED suitable for use is a P/N C395-XB290-E0400-X, manufactured by Cree, Inc., located in Durham, North Carolina, USA. Each LED 56 is bonded to substrate 52 using any

known bonding technique such as a conductive adhesive, solder, or eutectic bond. Each LED 56 is electrically connected to a power source (not shown) through a lead line 58 connected in a known manner to a wire bond pad 60 on substrate 52. In this embodiment, each row R(1), R(2), R(3) is electrically isolated by an isolation band 61. Each micro-reflector 54 includes a layer 62 of reflective and electrically conductive material both to reflect light from and to complete a circuit to electrically power an associated LED 56. Materials that are both optically reflective and electrically conductive and that can be bonded to electrically are limited to copper, aluminum, Au, and Ag, or combinations thereof. This construction provides micro-reflectors 54 that reflect light from an associated LED 56 and that are incorporated into the conductive circuitry to electrically power the associated LED 56.

Substrate 52 is preferably a 1-0-0 crystalline silicon wafer having defined crystallographic axes that are determined by silicon's crystalline lattice. One of the consequences of silicon's crystalline nature is that etching of silicon can be made to progress preferentially along some crystallographic axes as compared to others. As a result, when the surface of a silicon wafer is properly oriented, masked to expose the surface to be etched, and placed in an etching solution such as potassium hydroxide or hydrofluorid acid, openings are etched in the silicon having walls with a characteristic slope of about 54.7 degrees. Substrate 52 is fabricated using a cleaned and polished 1-0-0 silicon wafer. The wafer surfaces are super cleaned to remove all contamination. Cleaning can include a hydrofluoric acid soak followed by one or more aluminum hydroxide soaks, multiple dump rinses, and a distilled water spin rinse dry in heated dry nitrogen. A silicon nitride layer is applied with vapor deposition or plasma enhanced vapor deposition. This layer can be, for example, about 2,400 angstroms. The silicon nitride layer is then coated with photo resist on

top that is imaged or exposed with a negative mask. It is necessary to remove photo resist from wafers prior to etching into the silicon. An oxygen plasma (12cc/min. oxygen flow at 360 watts) or positive resist stripper (such as Shipley 1112 A) followed by several distilled water rinses can be used here. The unexposed photo resist is removed to expose the surface where openings that will become the micro-reflectors are desired. In one preferred embodiment, the silicon surface is prepared to expose a plurality of square shapes having sides measuring about 700 microns (0.028 in.) and spaced apart in a center-to-center spacing of about 800 microns (0.032 in.). The exposed portions of the silicon nitride layer are then etched. The silicon nitride can be etched with buffered hydrofluoric acid (BHF), which will not attach silicon. An alternative to BHF is reactive ion etch (RIE). One example of the RIE for this application is to etch for 90 seconds at 150 watts and 50 standard cubic centimeters per minute Sulfur Hexafluoride (SF_6) at 100 mTorr vacuum. The silicon nitride openings are etched until the base silicon wafer is fully exposed and shiny. The potassium hydroxide (KOH) is a wet etch that attacks silicon preferentially in the 1-0-0 plane producing a characteristic anisotropic V-etch with sidewalls that form a 54.7 degree angle with the surface (35.3 degree from the normal). The etch rate can be about 750 angstroms per minute at room temperature using a potassium hydroxide (KOH) solution of 400 grams of KOH per liter of distilled water. At 52 degrees C the etch rate is about 14 microns per hour. The speed of the etch can be adjusted by those skilled in the art. The etch rate of the silicon nitride layer is about 300 times slower than the etch rate of the silicon. It may be necessary to monitor and adjust the thickness of the silicon nitride layer to insure it is properly masking during the entire base silicon wafer etching. Adding 1 percent isopropyl alcohol to the KOH solution will lower the surface tension of the solution and usually results in smoother etched

walls. The result is a substrate 66 as seen in Figs. 7-9, having a densely packed array of openings 68. In this embodiment, openings 68 are arranged in a densely packed array in a center-to-center spacing of about 800 microns (0.032 in.). Each micro-reflector is formed in a truncated pyramidal shape in which opening 68 has sides have dimensions 70 of about 700 microns (0.028 in.) square. Openings 68 have sidewalls 72 that slope to a base 74 at an angle of about 54.7 degrees from a horizontal plane. Base 74 has a dimension 76 of about 346 microns (0.014 in.) square and openings have a depth (D) of about 250 microns (0.010 in.). These dimensions are merely illustrative and the invention is not limited to an optical device with these dimensions. For example, an optical device may be constructed and arranged so that the micro-reflectors have a center-to-center spacing of about 3 mm or less.

Substrate 52 is then metallized to provide several thin film layers. Preferably, the film layers are applied using a vapor deposition process or a plasma enhanced vapor deposition process known by those skilled in the art. First, a dielectric coating of about 1000 angstroms of silicon dioxide is applied to isolate the conductive circuit from the semiconductor. An adhesion layer of about 100-500 angstroms of titanium is then applied to improve adhesion of the metal layers. Next, a barrier metal layer of about 100-500 angstroms of nickel is applied to prevent metal migration between the layers. Finally, a light reflecting and electrically conducting layer is applied to form both an optical reflector and an electrical circuit. For UV light generation this layer can be about 1-10 microns of silver or aluminum, and for visible light the layer can be about 1-10 microns of gold. Another possible layer combination is to use 1,000 angstroms of silicon dioxide to isolate the conductive circuit followed by 1,000 angstroms of titanium to improve adhesion of the metal layers. A barrier layer of about 1,000 angstroms of nickel may be applied to prevent metal migration between

the layers. The nickel layer may then by coated with about 6 microns of silver to form the reflective and electrical conductive layer. The nickel and silver material have the additional advantage of being an electrical conductor lending themselves to common bonding techniques used for semiconductor devices such as wire bonding with Au, Ag, Al, thermal adhesives and soldering processes. The heavy silver layer helps to carry high electrical currents to optimize optical UV power generation. It is not desirable to use heavy nickel layers due to the tendency of the nickel to cause peeling of the metal.

After the metallization process, isolation band 61 is formed using known processes to form the electrical circuits on the metallized substrate. There are several known methods of forming circuits on metallized substrates. For example, one method is to use a laser to cut through the metal and slightly into the silicon. Another method is to apply photo resist to the substrate, expose the substrate with a glass mask, etch with either wet etch or plasma, and rinse off the photo resist. The laser process has the advantage of being flexible and easy to change the location and geometry. The glass mask process has the advantage of using existing silicon fabrication systems. However, either process may be suitable. Metallization on the back of the silicon provides for solder attach a supporting structure such as a heat sink (not shown), for example. The metallization may be a heavy silver layer. This silver layer can be replaced by a flash of gold to protect the nickel. The flash of gold keeps the nickel from oxidizing for improved solderability. The gold will go into solution in the solder. Minimizing the gold thickness will minimize cost while insuring the solderability and will minimize gold embrittlement potential in the solder joint connection between the substrate and the supporting structure. Once the substrate has

been fully processed the LEDs are mounted and bonded in a known manner discussed above to complete the LED array.

The LED array 50 provides an improved collection and collimation of light emitted from the LEDs. Figure 10 shows a graphic illustration of improved directionality in which curve 80 represents assumed angular irradiance distribution of an LED without the use of optics. Curve 82 represents the angular distribution of the same LED after mounting into a micro-reflector formed by anisotropic etching 350 microns deep in a silicon substrate. Figure 11 is a graphic illustration showing the calculated power as a function of distance for an array of LEDs mounted in the substrate arranged in a grid with a 1 mm center-to-center spacing. As seen by comparing the graphic illustrations of Fig. 2 and Fig. 7, the optical power density of LED arrays without reflectors drops by about 50% at a distance of only about 0.5 cm (Fig. 2). However, the optical power density of the LED array of the present invention using the micro-reflectors drops by about 50% at a further distance of about 2.6 cm. Therefore, the LED array of the present invention can be located further away from the work surface while maintaining a relatively high optical power density.

Although the etched micro-reflectors in Figs. 7-9 are shown as having an inverted truncated pyramidal shape other shapes may be used. For example, Fig. 12 shows a substrate 84 formed with an array of micro-reflectors 86 having a parabolic shape. An LED 88 is mounted in each micro-reflector as discussed above so that light from each LED 88 is reflective by layer 90. Layer 90 is both a reflective and electrically conductive layer as discussed above. Micro-reflectors 86 may be machined, stamped, cast, or hot forged into a silicon substrate or other thermally conductive material such as copper. Copper, copper tungsten, aluminum, or other metals can be used if a dielectric layer is added over the top of the pocketed base

material prior to metallizing as described above for the silicon process. The base material can also be used as a return electrode if it is conductive. Alternatively, the base material can be a source electrode. Alternatively, parabolic micro-reflectors may be formed by a combination of etching and machining. For either process, machining may be achieved by known laser and plasma techniques.

The present invention provides for an alternative method of manufacturing an array module in which a substrate material is first metallized. Electrical circuits are then structured on the metallized substrate and the substrate is then etched for form openings. The openings are then metallized to form micro-reflectors that both reflects light and electrically powers a semiconductor device. This has the advantage of allowing fine features to be formed in the electrical circuit separately from the etching and plating tasks associated with forming the openings.

Figure 13 shows another embodiment in which a plurality of micro-reflectors may be formed by a combination of etching and machining. Substrate 92 is formed with a plurality of micro-reflectors 94 wherein substrate 92 is first etched to form openings 96 in a manner discussed above with reference to Figs. 7-9. A layer of reflective and electrically conductive material 98 is applied to substrate 92 and micro-reflectors 94 having a parabolic shape are machined in each opening 96. A plurality of LEDs 100 are then mounted within the micro-reflectors 94 in the manner discussed above.

In another embodiment as seen in Fig. 14, directionality of light can be further improved by molding or aligning a microlens array 102 over an LED array 104 similar to those of Figs. 7-9, 12, and 13. In this embodiment, each microlens 106 is associated with a micro-reflector 108 to further collect and collimate light from an associated LED 110. One type of microlens array is shown and described in PCT

Appl. No. PCT/US04/36370, filed November 1, 2004, the contents of which are hereby incorporated by reference in its entirety for all purposes.

Persons skilled in the art will recognize that many modifications and variations are possible in the details, materials, and arrangements of the parts and actions which have been described and illustrated in order to explain the nature of this invention and that such modifications and variations do not depart from the spirit and scope of the teachings and claims contained therein.

WHAT IS CLAIMED:

1. An optical array module, comprising:

a plurality of semiconductor devices mounted on a thermal substrate formed with a plurality of openings that function as micro-reflectors, wherein each semiconductor device is associated with a micro-reflector, each micro-reflector including a layer of reflective and conductive material to reflect light and to electrically power its associated semiconductor device.

2. The optical array module of claim 1, wherein the micro-reflectors are arranged in an array having a center-to-center spacing of about 3 mm or less.

3. The optical array module of claim 1, wherein each micro-reflector has a depth of about 250 microns (0.010 in.) or less.

4. The optical array module of claim 1, wherein each micro-reflector is formed in a truncated pyramidal shape.

5. The optical array module of claim 4, wherein each micro-reflector is formed as a substantially squared opening in a surface of the substrate with sidewalls that slope to a base.

6. The optical array module of claim 1, wherein each micro-reflector is formed having a parabolic shape.

7. The optical array module of claim 1, further including an array of micro-lenses so that each micro-lens is associated with a micro-reflector to further collect and collimate light from an associated semiconductor device.

8. The optical array module of claim 5, wherein the sidewalls slope at an angle of about 54.7 degrees from a horizontal plane.

9. The optical array module of claim 1, wherein the substrate is formed from one of silicon, SiC, diamond, AlN, Al203, or BeO.

10. The optical array module of claim 1, wherein each semiconductor device has a height and each opening has a depth, the height of each semiconductor device being substantially equal to the depth of each opening.

11. A method of manufacturing an optical array module, comprising:

providing a substrate,

forming a plurality of openings in the substrate,

providing a layer of reflective and electrically conductive material in each opening, and

mounting a semiconductor device within each opening so that the layer of reflective and electrically conductive material in each opening reflects light and electrically powers from its associated semiconductor device.

12. The method of claim 11, wherein the openings in the substrate are formed by a crystallographic etching process.

13. The method of claim 12, wherein the openings have sidewalls having a characteristic slope.

14. The method of claim 13, wherein the sidewalls slope at an angle of about 54.7 degrees.

15. The method of claim 11, wherein the openings in the substrate are formed by a machining process.

16. The method of claim 15, wherein the openings have a parabolic shape.

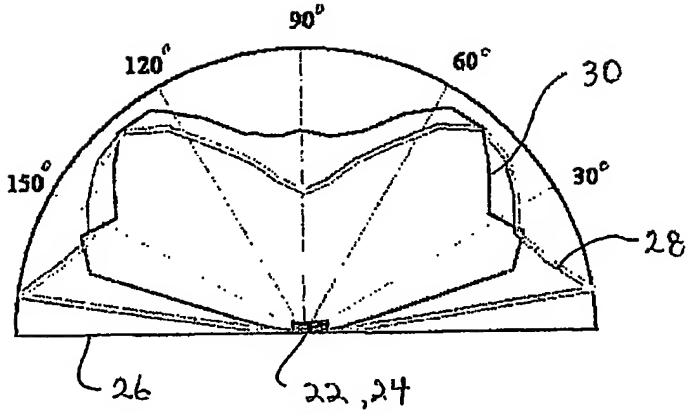
17. The method of claim 11, wherein the openings are formed in an array having a center-to-center spacing of about 800 microns (0.032 in.).

18. The method of claim 11, wherein the substrate is formed from one of silicon, SiC, diamond, AlN, Al203, or BeO.

19. The method of claim 11, wherein each semiconductor device has a height and each opening has a depth, the height of each semiconductor device being substantially equal to the depth of each opening.

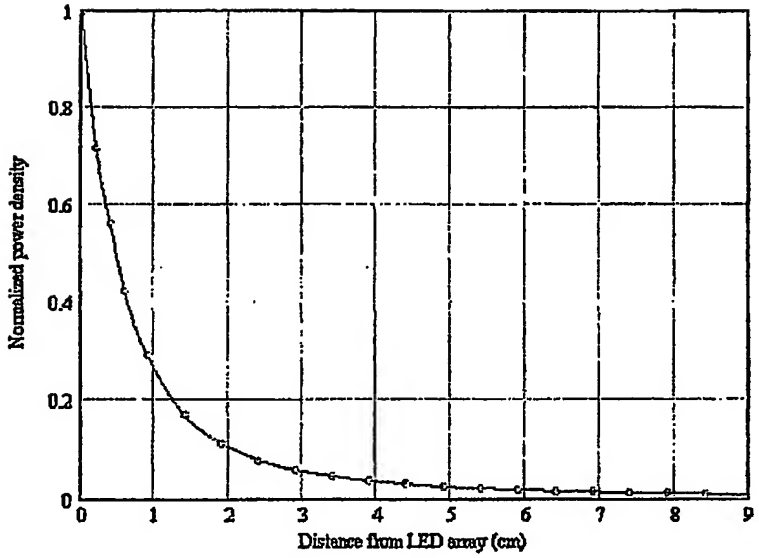
20. The method of claim 12, wherein each micro-reflector is formed in a truncated pyramidal shape.

Fig. 1



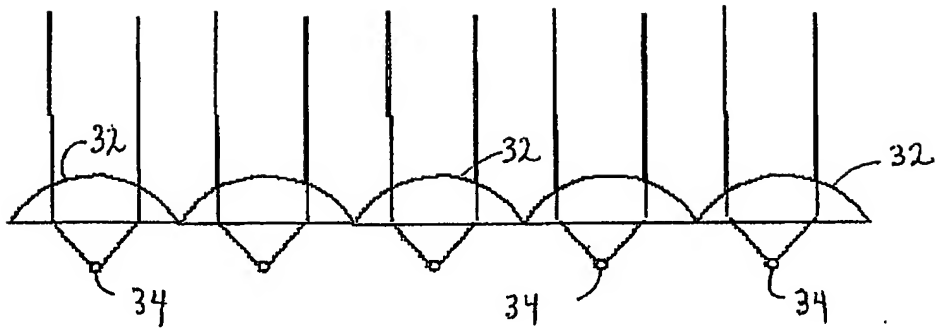
PRIOR ART

Fig. 2



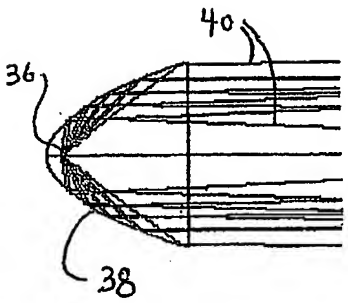
PRIOR ART

Fig. 3



PRIOR ART

Fig. 4



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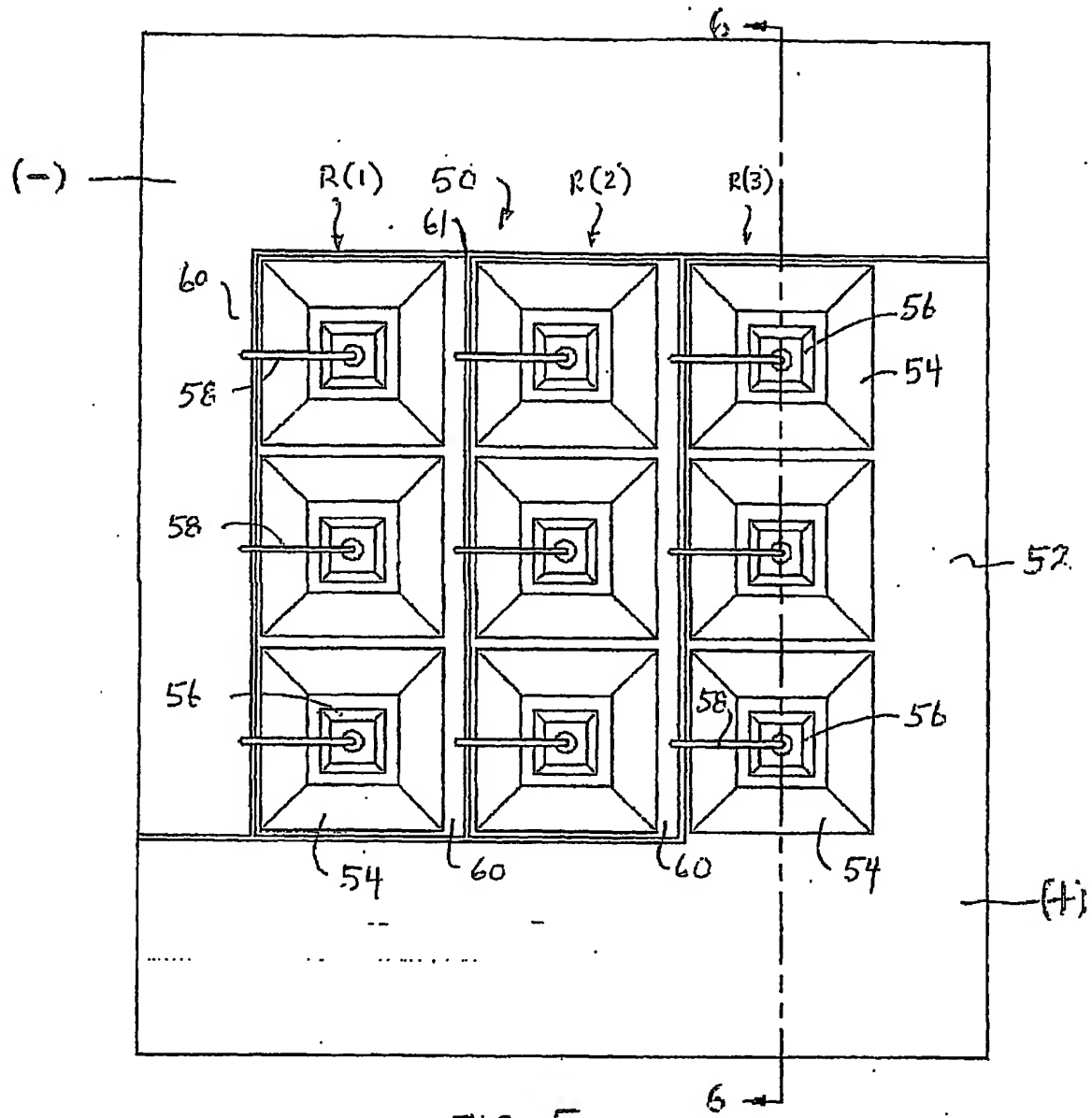
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(-)
R(1)
50
R(2)
R(3)
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56
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(+)
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FIG. 5

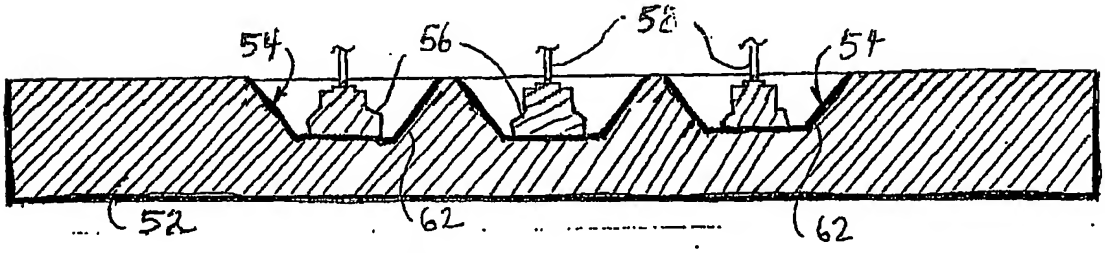
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FIG. 6

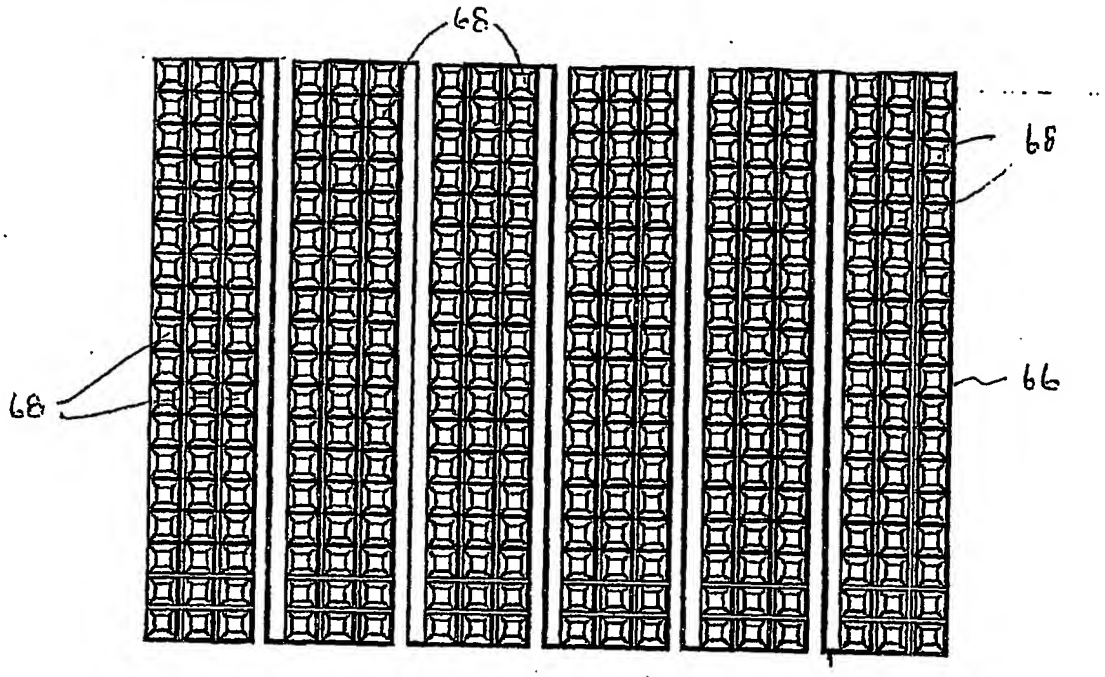


FIG. 7

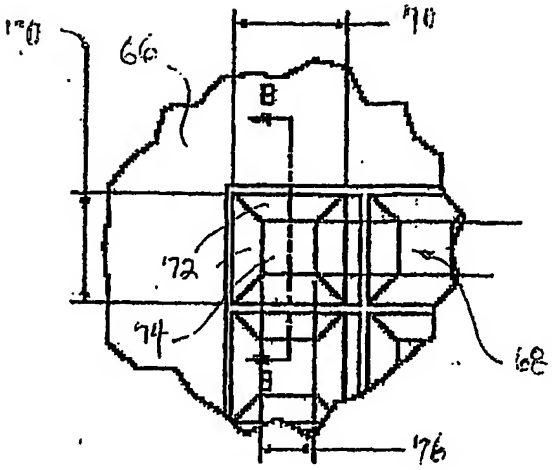


FIG. 8

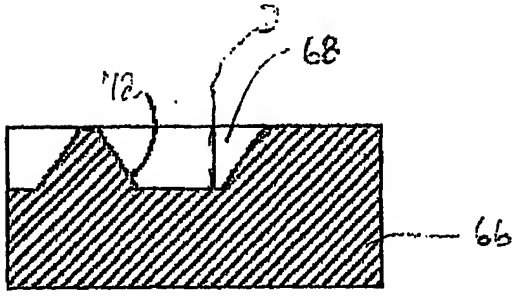


FIG. 9

Fig. 10

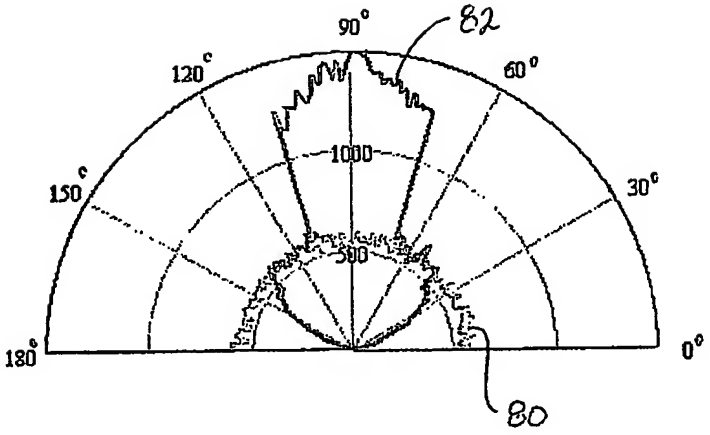
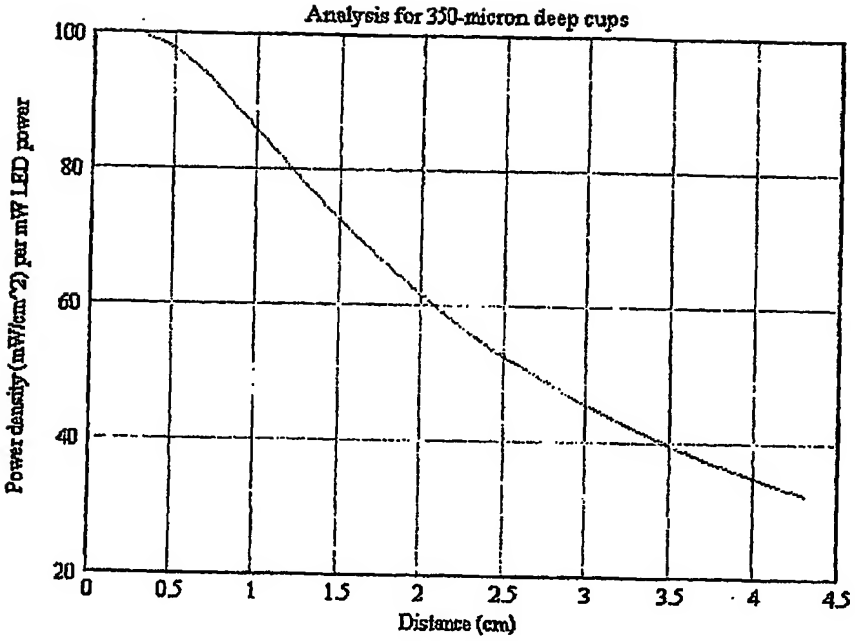


Fig. 11


Analysis for 350-micron deep cups
Power density (mW/cm^2) per mW LED power
100
80
60
40
20
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
Distance (cm)

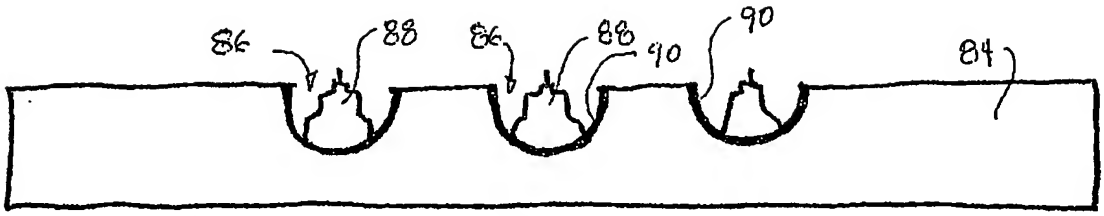


FIG. 12

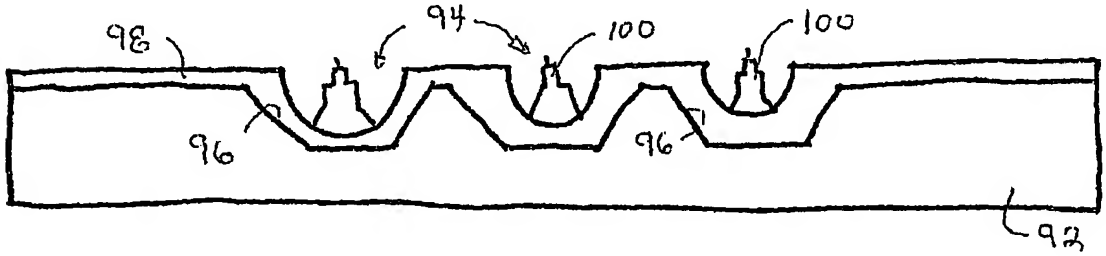


FIG. 13

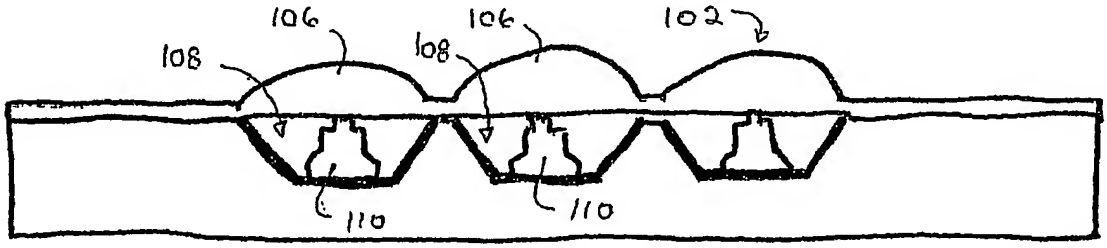


FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/09407

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01L 33/00
US CL : 257/88, 89, 95, 98, 99, 100
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/88, 89, 95, 98, 99, 100

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,418,384 (YAMANA et al.) 23 MAY 1995, column 2, line 45 to column 4, line 46.	1, 6, 11 --- 2, 3, 7, 10, 15-17, 19
X --- Y	US 5,003,357 (KIM et al.) 26 March 1991, column 1, line 23 to column 2, line 56.	1, 9, 11-13, 18 --- 4, 5, 8, 14, 20
Y	US 6,578,989 (OSUMI et al.) 17 June 2003, column 17, lines 43-64.	7

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 July 2005 (26.07.2005)	26 AUG 2005
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner of Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Steven Loke Telephone No. (571) 272-1657

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

PCT/US05/09407

Continuation of B. FIELDS SEARCHED Item 3:
EAST
search terms: semiconductor, light, reflect, recess, open, groove, trench, array, LED, light emitting device